

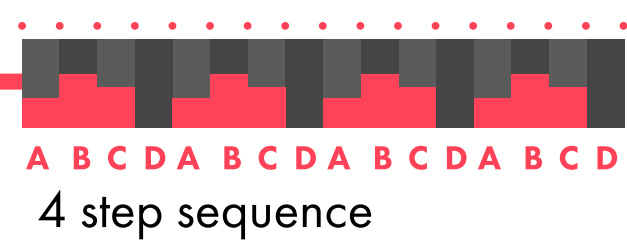
1/2

Set up 3 sequences of 4 steps
The second one is driven by a clock divider fed by the last step of the first sequence
The third one is driven by the last step of the second sequence



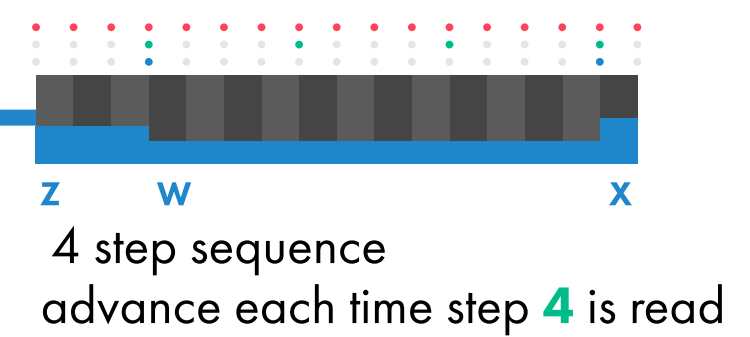
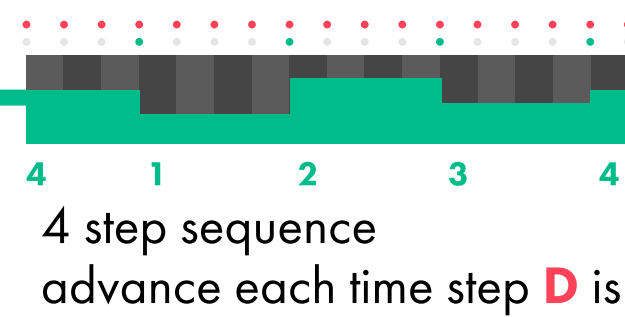
master clock
(square lfo)

gate emitted each
time this stage is read

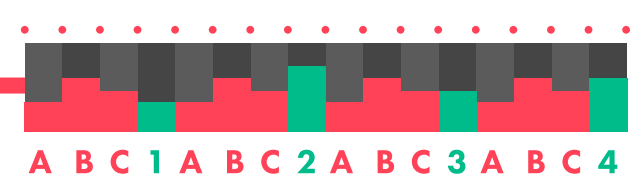
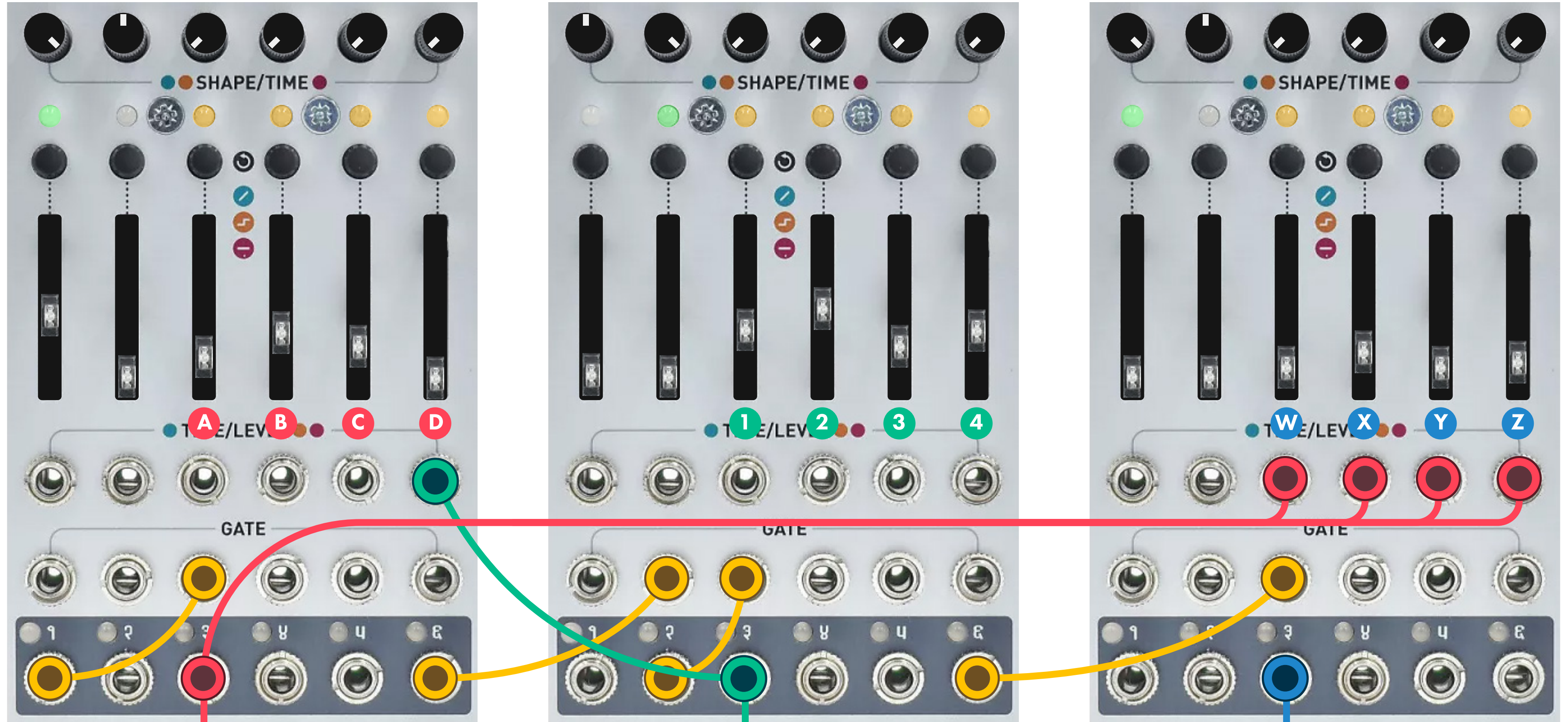


clock divider 1/2
(clocked square lfo)

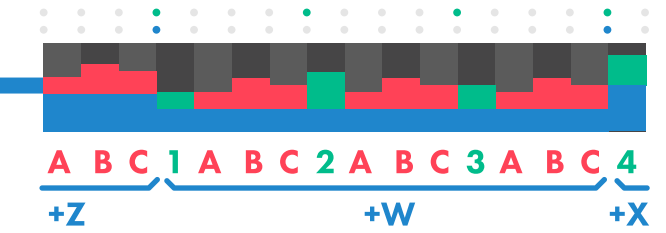
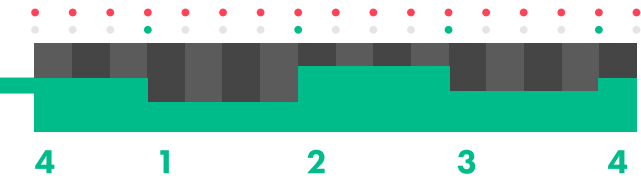
gate emitted each
time this stage is read



Use second sequence to modulate the last step of the first sequence and create a 32 step loop
Send the first sequence in each level input of the third sequence and create a 128 step loop



sequence **1234**
is modulating step **D**



This group becomes a sequential switch with 4 copies of **ABC1**
Each copies is read with a different offset according to fader **WXYZ**